Pharos™ III

- Most complete ADSL 2/2+/2++ chipset
- On-chip memory for increased Impulse noise protection and Interleaver depth for video and IPTV applications
- Dual Latency and DRR for triple play QoS
- SRA for robust connections
- SELT/DELT for line qualification and test
- Low power modes for power efficiency
- Double upstream with Annex M support
- Quad technology for bit rates up to 50 Mbps downstream and 5.5 Mbps upstream

the edge in broadband™

The Pharos™ III chipset is a high integration; high-performance, longest reach 12-port solution for low-power, high-density, ATU-C line card applications. Based on many years of high performance ADSL technology deployment around the world, Pharos III chipset offers the next generation ADSL for the emerging IPTV triple play markets. With added features such as INP up to 16 and interleaver depth D up to 511, Pharos III offers a distinct advantage for deploying Video on demand and IPTV applications.

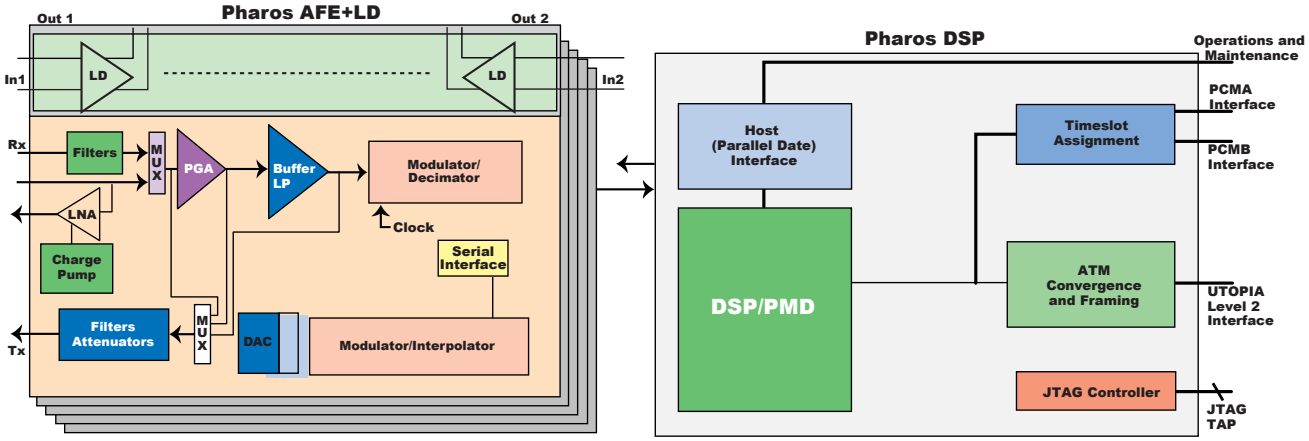
Consisting of a single monolithic 12-port digital processor and an integrated 2-port AFE (analog front-end) with line drivers, the Pharos III chipset provides a low chip-count solution for high-density line cards for IPDSLAM, MTU/MDU, DLC, and SAP equipment. The digital processor provides programmability and high-performance for future proof line card solutions. The AFE, in addition to integrating line drivers, incorporates external filters and other discrete components

Pharos III incorporates multiple interfaces and the Centillium Communications eXtremeDSL^{MAX}™ technology, making it the solution of choice for high-speed, multi-service line card platforms catering to derived voice and video services applications. The Pharos III chipset provides a low chip-count solution for high-density line cards. The digital processor provides programmability and high-performance for future proof line card solutions. The AFE incorporates external discrete components resulting in a reduced system BOM (bill of materials). It's high-resolution analog-to-digital and digital-to-analog converter circuits provide the performance required for high data rate applications.

Features

- Highly optimized 12-port, multi-mode ADSL, ADSL2, ADSL2+ and ADSL2++ (quad-spectrum mode) chipset
- Fully supports ADSL2 training/framing (ADSL2 feature set is backwards compatible with ADSL)
- Compliance with the following ITU-T specifications:
  - G.992.1 (ADSL G.dmt) with associated annexes
  - G.992.2 (ADSL G.lite) with associated annexes
  - G.992.3 (ADSL2) with focus on ADSL over POTS, and ADSL over ISDN
  - G.992.5 (ADSL2+) with associated annexes
  - ITU-T G.994 (G.hs)
  - ITU-T G.997.1 (G.ploam)
- High-performance ADSL engine supports the following loop profiles
- ADSL2+ peak rates of 1.3 Mbps single upstream and 25 Mbps downstream for short/medium loops with high-bit loading capability

Block Diagram



CENTILLIUM COMMUNICATIONS

Pharos™ III

Features Continued

- ADSL2/2+ Annex M upstream rates of 3.0 Mbps
- Long reach ADSL2 that supports 128 Kbps symmetrical up to 26,000 feet
- ADSL2++ peak rates of 5.5 Mbps upstream and 50 Mbps downstream for short/medium loops with high-bit loading capability
- Low-power chipset solution based on state-of-the-art process geometry
- IN-SS (intelligent spectrum selection) algorithm that optimally switches the PSD mask based upon the loop profile
- LA-SRA (loop adaptive seamless rate adaptation) that dynamically maintains link integrity despite changing noise conditions in the loop
- IN-LM (intelligent link management) feature suite that assists service providers in automating fault detection and the recovery aspect of OM (operation and maintenance)
- Low component count for CO hybrid based on high level of front-end integration for Annex A/B combination line cards
- Supports IN-MCP (intelligent multi-channel payload) that enables simultaneous transport of different traffic types (dual-latency)
- Supports the eXtremeDSL^{MAX} technology and feature set for high data rate and long reach
- Less than 1 square inch per port of PCB area (from UTOPIA to tip and ring)
- Per channel feature provisioning capability
- Echo cancellation capability for optional spectrum overlap operation
- Upstream Viterbi and transmit widowing
- ATM cell header compression
- Pin-to-pin compatible with existing Pharos chipset
- F/W, S/W compatible to Pharos chipset

Digital Processor (DSP)

- 12-port ADSL DSP chip
- Single, low-cost external crystal operation
- Programmable core for software upgrades
- No external memory required (on-chip interleaver)
- UTOPIA Level 2, 50 MHz interface for ATM data transfer
- Glue less interface to various host processors
- Extended UTOPIA addressing supports up to 255 PHYs without any additional external logic
- JTAG (IEEE 1149.1) boundary scan
- 16-bit host interface
- Muxed and non-muxed address modes
- Per channel operation of all features

Analog Front End/Line Driver

- Two-port, high-resolution, low-power AFE and line driver
- Complete AFE for ADSL CO line cards
- Low-power ± 12V line driver
- Single 3.3V supply with on-chip regulator for 1.8V logic supply and charge pump for 5.25V LNA (low noise amplifier) supply
- Receive programmable gain from 0 dbm to 30 dbm in 1.5 dbm steps
- Integrated Annex B and billing tone high-pass filter
- Low-noise pre-amplifier with programmable gain from -6 dbm to 9 dBm in 3 dBm steps
- Digital interface at 35.328 MHz on two wires (double data rate mode for ADSL2++)

Pharos III Chipset Options

Product	Function	Part Number	Package
Pharos III, Annex A/B, ADSL2/2+	Digital Chip (DSP)	CT59DC12-PM-AA	456-PIN PBGA
	Analog Chip (AFE)	CT56AC02-QA-BB	108-PIN QFN
Pharos III, Annex A/B, ADSL2/2+/2++	Digital Chip (DSP)	CT89DC12-PM-AA	456-PIN PBGA
	Analog Chip (AFE)	CT56AC02-QA-BB	108-PIN QFN
Pharos III, Annex C, ADSL2/2+/2++	Digital Chip (DSP)	CT79DC12-PM-AA	456-PIN PBGA
	Analog Chip (AFE)	CT56AC02-QA-BB	108-PIN QFN

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